## CLAIMS

**WHAT IS CLAIMED:**

1. A semiconductor device, comprising:

a bulk substrate;

a multiple thickness buried oxide layer formed above said bulk substrate; and

an active layer formed above said multiple thickness buried oxide layer, said semiconductor device being formed in said active layer above said multiple thickness buried oxide layer.

2. The device of claim 1, wherein said bulk substrate is comprised of silicon.

3. The device of claim 1, wherein said semiconductor device is a transistor.

4. The device of claim 1, wherein said semiconductor device is part of at least one of a microprocessor, a memory device and a logic device.

5. The device of claim 1, wherein said active layer is comprised of silicon.

6. The device of claim 1, wherein said active layer has a thickness ranging from approximately 5-30 nm.

7. The device of claim 1, wherein said buried oxide layer is comprised of silicon dioxide.

8. The device of claim 1, wherein said multiple thickness buried oxide layer comprises:

a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections.

9. The device of claim 1, wherein said semiconductor device is a transistor having a channel region, at least a portion of said channel region being positioned above a section of said buried oxide layer that has a thickness that is less than a thickness of a remaining portion of said buried oxide layer.

10. The device of claim 1, wherein said semiconductor device is a transistor comprised of a gate electrode and wherein said multiple thickness buried oxide layer has a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than a thickness of said second sections, said first section being at least partially positioned under said gate electrode.

11. The device of claim 1, wherein said semiconductor device is a transistor comprised of a gate electrode and wherein said multiple thickness buried oxide layer has a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than a thickness of said second sections, said first section being substantially aligned with said gate electrode.

12. The device of claim 8, wherein said first section has a thickness ranging from approximately 30-50 nm and said second sections have a thickness ranging from approximately 120-180 nm.

13. A transistor, comprising:

a bulk substrate;

a buried oxide layer formed above said bulk substrate, said buried oxide layer comprising a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections; and

an active layer formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer.

14. The device of claim 13, wherein said bulk substrate is comprised of silicon.

15. The device of claim 13, wherein said transistor is part of at least one of a microprocessor, a memory device and a logic device.

16. The device of claim 13, wherein said active layer is comprised of silicon.

17. The device of claim 13, wherein said active layer has a thickness ranging from approximately 5-30 nm.

18. The device of claim 13, wherein said buried oxide layer is comprised of silicon dioxide.

19. The device of claim 13, wherein said transistor comprises a channel region, at least a portion of said channel region being positioned above at least a portion of said first section of said buried oxide layer.

20. The device of claim 13, wherein said transistor comprises a gate electrode and wherein said first section of said buried oxide layer is at least partially positioned under said gate electrode.

21. The device of claim 13, wherein said transistor comprises a gate electrode and wherein said first section of said buried oxide layer is substantially aligned with said gate electrode.

22. The device of claim 13, wherein said first section has a thickness ranging from approximately 30-50 nm and said second sections have a thickness ranging from approximately 120-180 nm.

23. A transistor comprised of a channel region, said transistor comprising:

a bulk silicon substrate;

a buried oxide layer formed above said bulk silicon substrate, said buried oxide layer comprising a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness,

said thickness of said first section being less than said thickness of said second sections; and

an active layer formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer, at least a portion of said channel region being positioned above said first section of said buried oxide layer.

24. The device of claim 23, wherein said transistor is part of at least one of a microprocessor, a memory device and a logic device.

25. The device of claim 23, wherein said active layer is comprised of silicon.

26. The device of claim 23, wherein said active layer has a thickness ranging from approximately 5-30 nm.

27. The device of claim 23, wherein said buried oxide layer is comprised of silicon dioxide.

28. The device of claim 23, wherein said transistor further comprises a gate electrode and wherein said first section of said buried oxide layer is at least partially positioned under said gate electrode.

29. The device of claim 23, wherein said transistor further comprises a gate electrode and wherein said first section of said buried gate oxide layer is substantially aligned said gate electrode.

30. The device of claim 23, wherein said first section has a thickness ranging from approximately 30-50 nm and said second sections have a thickness ranging from approximately 120-180 nm.

31. A method of forming a semiconductor device, comprising:

performing a first oxygen ion implant process on a silicon substrate;

forming a masking layer above said substrate after said first oxygen ion implant process;

performing a second oxygen ion implant process on said substrate through said masking layer; and

performing at least one heating process on said substrate to form a multiple thickness buried oxide layer in said substrate.

32. The method of claim 31, further comprising forming a semiconductor device above said multiple thickness buried oxide layer.

33. The method of claim 31, wherein said first oxygen ion implant process is performed at an energy level ranging from approximately 10-40 keV and using an oxygen dopant dose ranging from approximately $10^{17}$-$10^{18}$ ions/cm$^2$.

34. The method of claim 31, wherein said second oxygen ion implant process is performed at an energy level ranging from approximately 30-150 keV and using an oxygen dopant dose ranging from approximately $10^{17}$-$10^{18}$ ions/cm$^2$.

35. The method of claim 31, wherein forming a masking layer above said substrate comprises forming a masking layer comprised of at least one of a photoresist material and a gate electrode above said substrate.

36. The method of claim 31, wherein performing at least one heating process comprises performing at least one heating process at a temperature ranging from approximately 950-1150°C.

37. The method of claim 31, wherein said multiple thickness buried oxide layer comprises:

a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections.

38. A method of forming a semiconductor device, comprising:

forming a masking layer above said substrate;

performing a first oxygen ion implant process on a silicon substrate through said masking layer;

removing said masking layer;

performing a second oxygen ion implant process on said substrate after said masking layer is removed; and

performing at least one heating process on said substrate to form a multiple thickness buried oxide layer in said substrate.

39. The method of claim 38, further comprising forming a semiconductor device above said multiple thickness buried oxide layer.

40. The method of claim 38, wherein said first oxygen ion implant process is performed at an energy level ranging from approximately 10-40 keV and using an oxygen dopant dose ranging from approximately $10^{17}$-$10^{18}$ ions/cm$^2$.

41. The method of claim 38, wherein said second oxygen ion implant process is performed at an energy level ranging from approximately 10-40 keV and using an oxygen dopant concentration ranging from approximately $10^{17}$-$10^{18}$ ions/cm$^2$.

42. The method of claim 38, wherein forming a masking layer above said substrate comprises forming a masking layer comprised of at least one of a photoresist material and a gate electrode above said substrate.

43. The method of claim 38, wherein performing at least one heating process comprises performing at least one heating process at a temperature ranging from approximately 950-1150°C.

44. The method of claim 38, wherein said multiple thickness buried oxide layer comprises:

a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections.

45. A method, comprising:

forming a layer of silicon dioxide above a first substrate;

forming a masking layer above a portion of said layer of silicon dioxide;

performing at least one etching process to etch a recess in said substrate adjacent each side of said masking layer;

removing said masking layer;

performing at least one of an oxidation process and a deposition process to form silicon dioxide in at least said recesses;

performing at least one chemical mechanical polishing operation on at least said silicon dioxide formed in said recesses;

bonding a second substrate to at least said silicon dioxide formed in said recesses; and

removing a portion of said second substrate.

46. The method of claim 45, wherein forming a layer of silicon dioxide above a first substrate comprises forming a layer of silicon dioxide above a first substrate by performing an oxidation process.

47. The method of claim 45, wherein forming a masking layer above a portion of said layer of silicon dioxide comprises forming a masking layer comprised of a photoresist material above a portion of said layer of silicon dioxide.

48. The method of claim 45, wherein performing at least one etching process to etch a recess in said substrate adjacent each side of said masking layer comprises performing at least one etching process to etch a recess having a depth ranging from approximately 10-50 nm in said substrate adjacent each side of said masking layer.